Emmanuel Vargas

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HW3 Single Cycle MIPS Architecture

1. In a single cycle CPU the clock period should be set to the worst instruction latency, so we have to calculate the latency for the following instructions:

Sub $rd, $rs, $rt

1. Fetch instruction using I-Mem – 40ps
2. Read the two registers – 80ps
3. Data passed to ALU by mux: 20ps
4. Compute in ALU: 100ps
5. Pass ALU result to mux: 20ps
6. Write ALU result to reg: 60ps

Total time: 320ps

Lw $rt, offset($rs)

1. Fetch instruction using I-Mem – 40ps
2. Read address from register – 80ps
3. Sign extend the offset – 20ps
4. Pass offset to ALU via mux – 20ps
5. Compute address in ALU – 100ps
6. Read at the address in D-mem – 200ps
7. Output of D-mem passes through mux – 20ps
8. Write to register – 60ps

Total: 540ps

The clock period should be set to 540ps because that is the time it takes to compute the longest instruction the processor handles, which is store word.

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   1. If we design a single cycle processor then the clock latency should be the sum of all the steps, as in the worst case all of those steps will be used for a single instruction and should therefore be the clock latency of the CPU.

100ps + 120ps + 220ps + 300ps + 120ps = 820ps.

* 1. In a pipelined processor the clock latency of the CPU should simply be the time of the longest stage in the pipeline, in this case we have 5 stages, IF, ID, EX, MEM and WB. The MEM stage takes the longest at 300ps, therefore the clock latency of this pipelined CPU should be 300ps.